Claims

1. Phase change memory (21, 41, 71, 81, 101, 161, 162, 215) comprising a memory material layer (23, 49, 93, 109, 179) consisting of a phase change material, and a first (25, 47, 73, 97, 115) and second (27, 51, 75, 97, 115) electrical contact which are located at a distance from one another and via which a switching zone (31, 61, 119, 177) of the memory material layer (23, 49, 93, 109, 179) can be traversed by a current signal, wherein the current signal can be used to induce a reversible phase change (11, 13) between a crystalline phase (3) and an amorphous phase (5) and thus a change in resistance (7) of the phase change material in the switching zone (31, 61, 119, 177),
characterized in that
the switching zone (31, 61, 119, 177) is located along a lateral extension (33, 45, 83) of the phase change memory between the first (25, 47, 73, 97, 115) and second (27, 51, 75, 97, 115) electrical contacts, wherein current conduction (35, 63, 77) of the current signal through the switching zone (31, 61, 119, 177) takes place along the lateral extension (33, 45, 83), and wherein the switching zone (31, 61, 119, 177) is located at a narrowing (65) between the first (25, 47, 73, 97, 115) and second (27, 51, 75, 97, 115) electrical contacts in the memory material layer (23, 49, 93, 109, 179), wherein a size (67, D) of the narrowing (65) is smaller than a size (69, 121) of the memory material layer (23, 49, 93, 109, 179) at the first (25, 47, 73, 97, 115) or second (27, 51, 75, 97, 115) electrical contact.

2. Phase change memory (21, 41, 71, 81, 101, 161, 162, 215) according to Claim 1,
characterized in that
a traversing surface area, formed perpendicularly to the lateral extension, for the current conduction (35, 63, 77) in the switching zone (31, 61, 119, 177) is narrowed

in relation to a traversing surface area for the current conduction (35, 63, 77) at the first (25, 47, 73, 97, 115) or second (27, 51, 75, 97, 115) electrical contact, wherein the ratio of the traversing surface areas lies between 1:2 and 1:100.

3. Phase change memory (41, 71) according to Claim 1 or 2,
characterized in that
a size (67) of the narrowing (65) in the lateral extension (45) is smaller than a size (69) of the memory material layer (49) in the lateral extension (45) at the first (47, 49) or second (51, 75) electrical contact.

4. Phase change memory (101) according to any of Claims 1 to 3,
characterized in that
a size (D) of the narrowing in the vertical extension (85) is smaller than a size (121) of the memory material layer (109) in the vertical extension (85) at the first or second electrical contact (115).

5. Phase change memory (21, 41, 71, 81, 101, 161, 162, 215) according to any of Claims 1 to 4,
characterized in that
the first (25, 47, 73, 97, 115) and/or second (27, 51, 75, 97, 115) electrical contacts directly adjoin the memory material layer (23, 49, 93, 109, 179) and the switching zone (31, 61, 119, 177) is formed in the memory material layer (23, 49, 93, 109, 179) at a distance (79) from the first (25, 47, 73, 97, 115) and/or second (27, 51, 75, 97, 115) contact.

6. Phase change memory (41, 161, 162, 215) according to any of Claims 1 to 5,
characterized in that
the distance between the first (47, 163) and second (51, 175) electrical contact is oriented along the lateral

extension (45), wherein the first electrical contact (47, 163) is located below the memory material layer (49, 179) and the second electrical contact (51, 175) is located above the memory material layer (49, 179).

7. Phase change memory (71, 81, 101) according to any of Claims 1 to 5,
characterized in that
the distance between the first (73, 97, 115) and second (75, 97, 115) electrical contact is oriented along the lateral extension (83), wherein the first (73, 97, 115) and the second (75, 97, 115) electrical contacts are located above the memory material layer (93, 109).

8. Phase change memory (21, 41, 71, 81, 101, 161, 162, 215) according to Claim 6 or 7,
characterized in that
the switching zone (31, 61, 119, 177) is located in a region between the first (25, 47, 73, 97, 115) and second (27, 51, 75, 97, 115) electrical contact and below the first (25, 47, 73, 97, 115) and above the second (27, 51, 75, 97, 115) or above the first (25, 47, 73, 97, 115) and below the second (27, 51, 75, 97, 115) electrical contact along the lateral extension (33, 45, 83).

9. Phase change memory (41, 71) according to any of Claims 1 to 8,
characterized in that
a core forming zone (55) directly adjoins the memory material layer (49).

10. Phase change memory (21, 41, 71, 81, 101, 161, 162, 215) according to any of Claims 1 to 9,
characterized in that
the first (25, 47, 73, 97, 115) and second (27, 51, 75, 97, 115) electrical contacts and the memory material layer (23, 49, 93, 109, 179) form part of a MESA structure (89, 103) which is applied to a substrate (87,

105, 169), wherein the memory material layer (23, 49, 93, 109, 179) is insulated from a heat sink (87, 105, 181) by a thermal barrier (91, 107, 183).

11. Phase change memory assembly (131) comprising one or more phase change memories (21, 41, 71, 81, 101, 161, 162, 215) according to any of Claims 1 to 10,
characterized in that
in each case one of the electrical contacts (139, 141, 143) of each phase change memory (133, 135, 137) lies at the same electrical potential (147) as a respective one of the electrical contacts (139, 141, 143) of the other phase change memories.

12. Phase change memory cell (167, 187, 203) comprising a phase change memory (21, 41, 71, 81, 101, 161, 162, 215) according to any of Claims 1 to 10 and/or a phase change memory assembly (131) according to Claim 11,
characterized by
a selection unit (165, 191) with a non-linear current/voltage characteristic.

13. Phase change memory cell (167, 187, 203) according to Claim 12,
characterized in that
the selection unit (165, 191) is integrated in the phase change memory (162) and/or the phase change memory assembly.

14. Phase change memory cell (167, 187, 203) according to Claim 13,
characterized in that
the selection unit (165, 191) is located in the phase change memory (162) between the memory material layer (179) and the first electrical contact (163) and/or between the memory material layer (179) and the second electrical contact (175).

15. 2D phase change memory cell array (201, 213) characterized by
a number of two-dimensionally connected and individually addressable phase change memory cells ((167, 187, 203)) according to any of Claims 12 to 14.

16. 3D phase change memory cell array (211) comprising a number of 2D phase change memory cell arrays (201, 213) according to Claim 15 which are arranged one above the other,
characterized in that
respective phase change memories (215) which are arranged directly above one another are contacted by way of a common via (219).

17. 3D phase change memory cell array (211) according to Claim 16,
characterized in that,
in order to address a selected phase change memory (215) of a 2D phase change memory cell array (213), respective phase change memories (215) which are arranged directly above one another can be switched to a first potential by way of the common via (219), and in the process all the other phase change memory cells of any other 2D phase change memory cell array (213) can be switched to a second potential (221).

18. Electronic component (225) with an application-specific module (227) and an integrated memory function and/or logic function (223), comprising a phase change memory (21, 41, 71, 81, 101, 161, 162, 215) according to any of Claims 1 to 10 and/or a phase change memory assembly (131) according to Claim 11 and/or a phase change memory cell (167, 187, 203) according to any of Claims 12 to 14 and/or a phase change memory cell array (201, 213, 211) according to any of Claims 15 to 17.